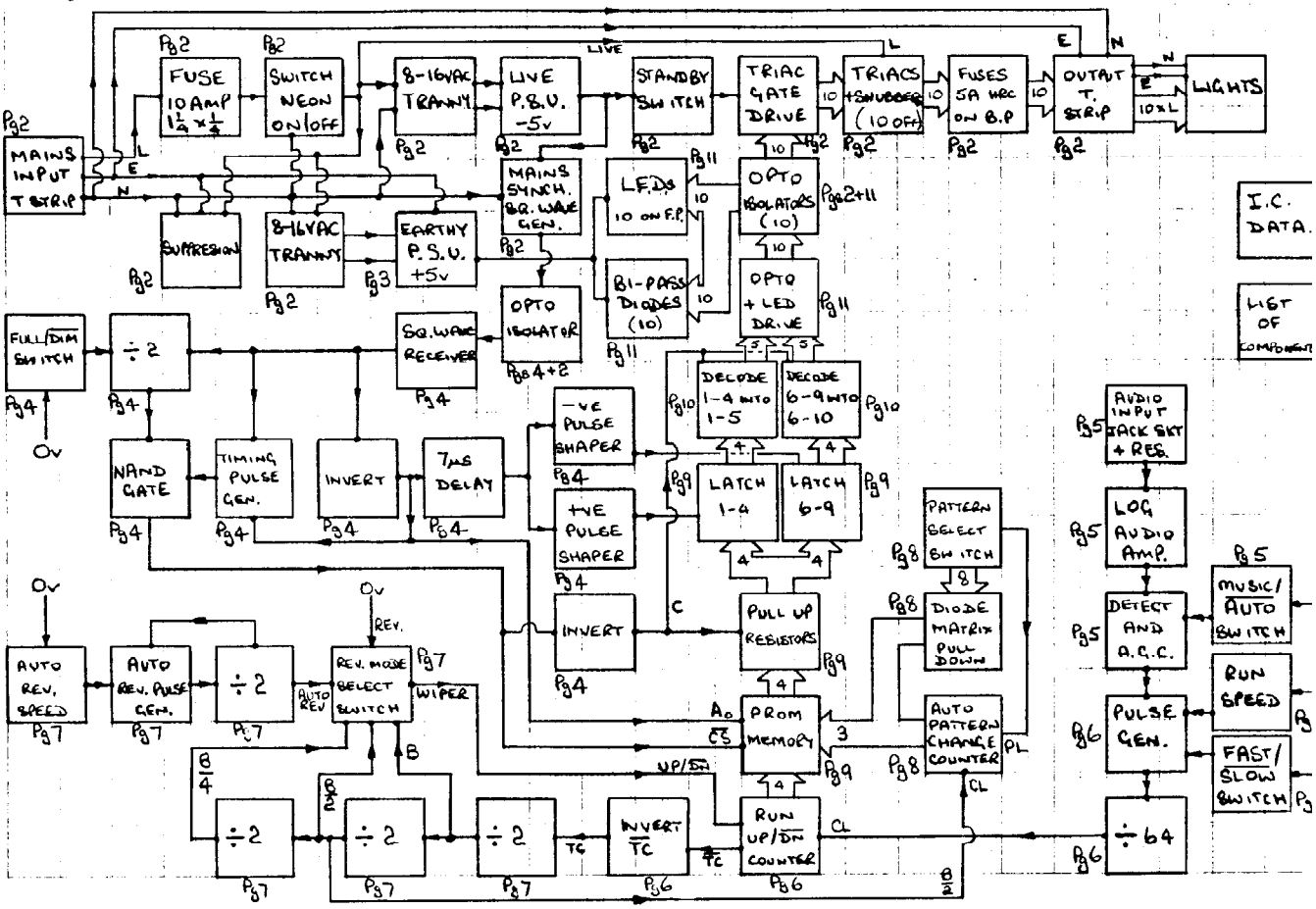
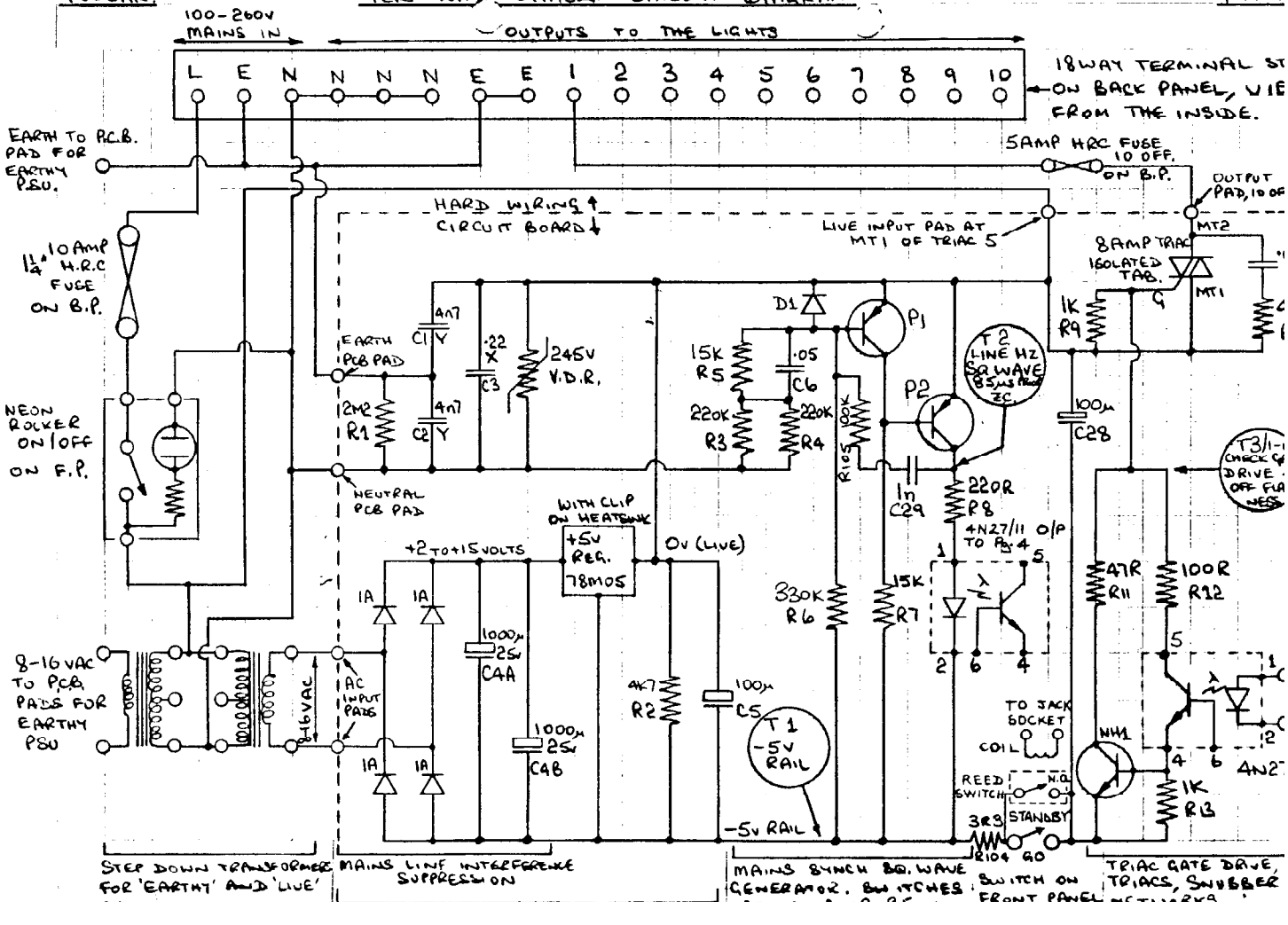
PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM — P.F.M.

BLOCK DIAGRAM



MK III NOV 79. Pg8, 3×27K→3×2K2; 8×220R→LINKS.
Pg6+7, Comp VALUE CHANGES IN PULSE GENERATORS.

PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM — P.F.M.

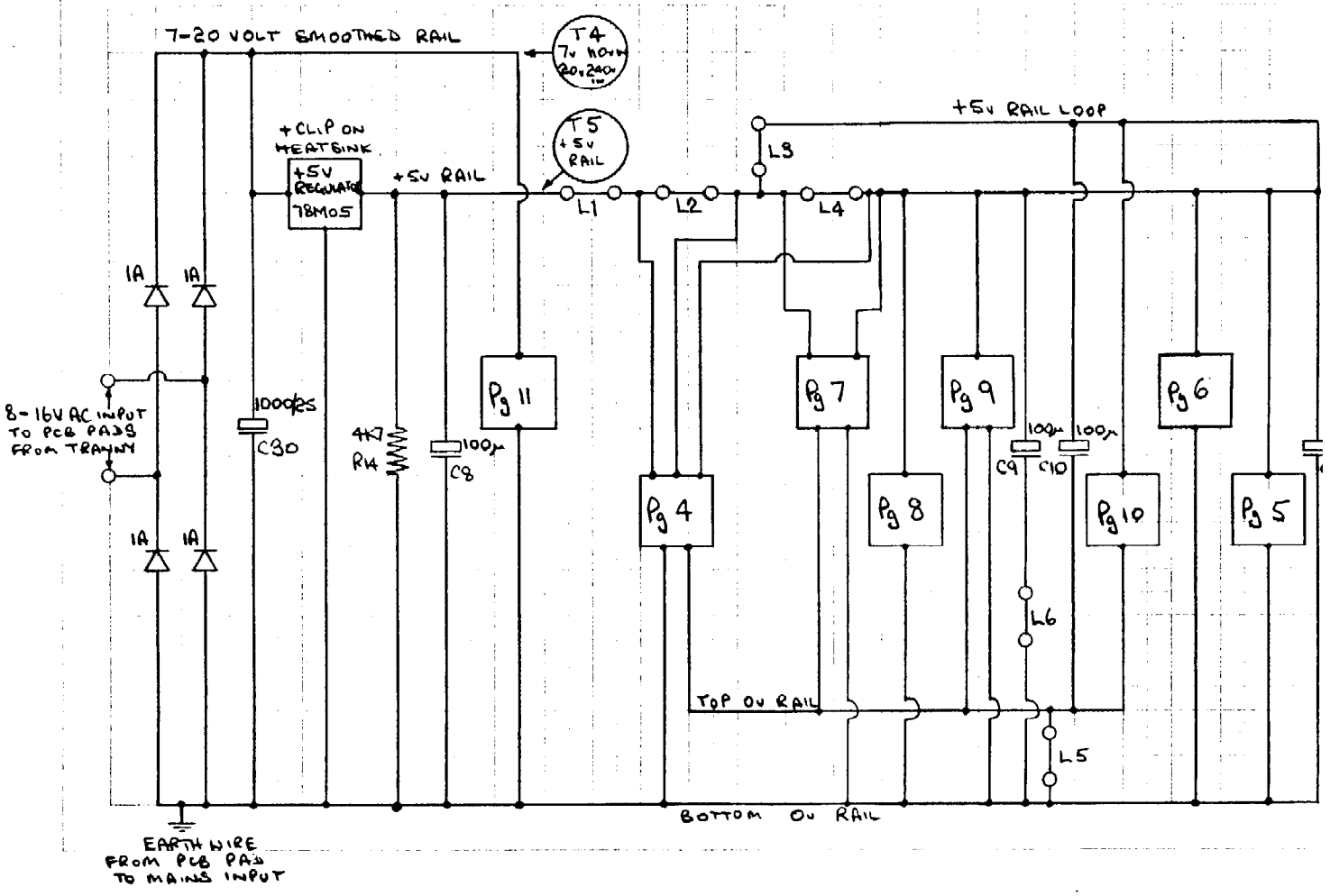


PULSAR

TEN WAY CHASER CIRCUIT DIAGRAM

P.F.M.

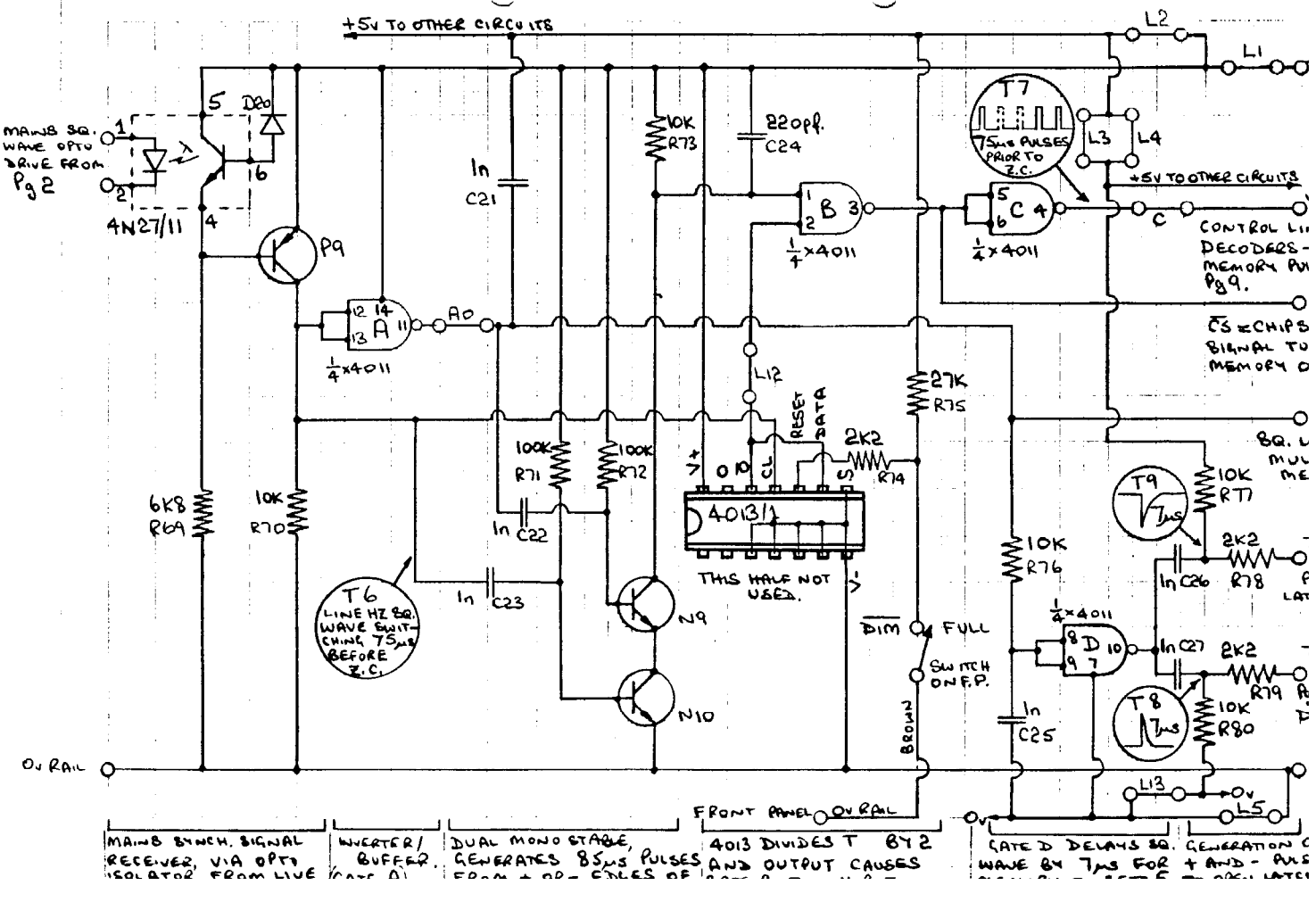
RAIL CONNECTIONS



PULSAR

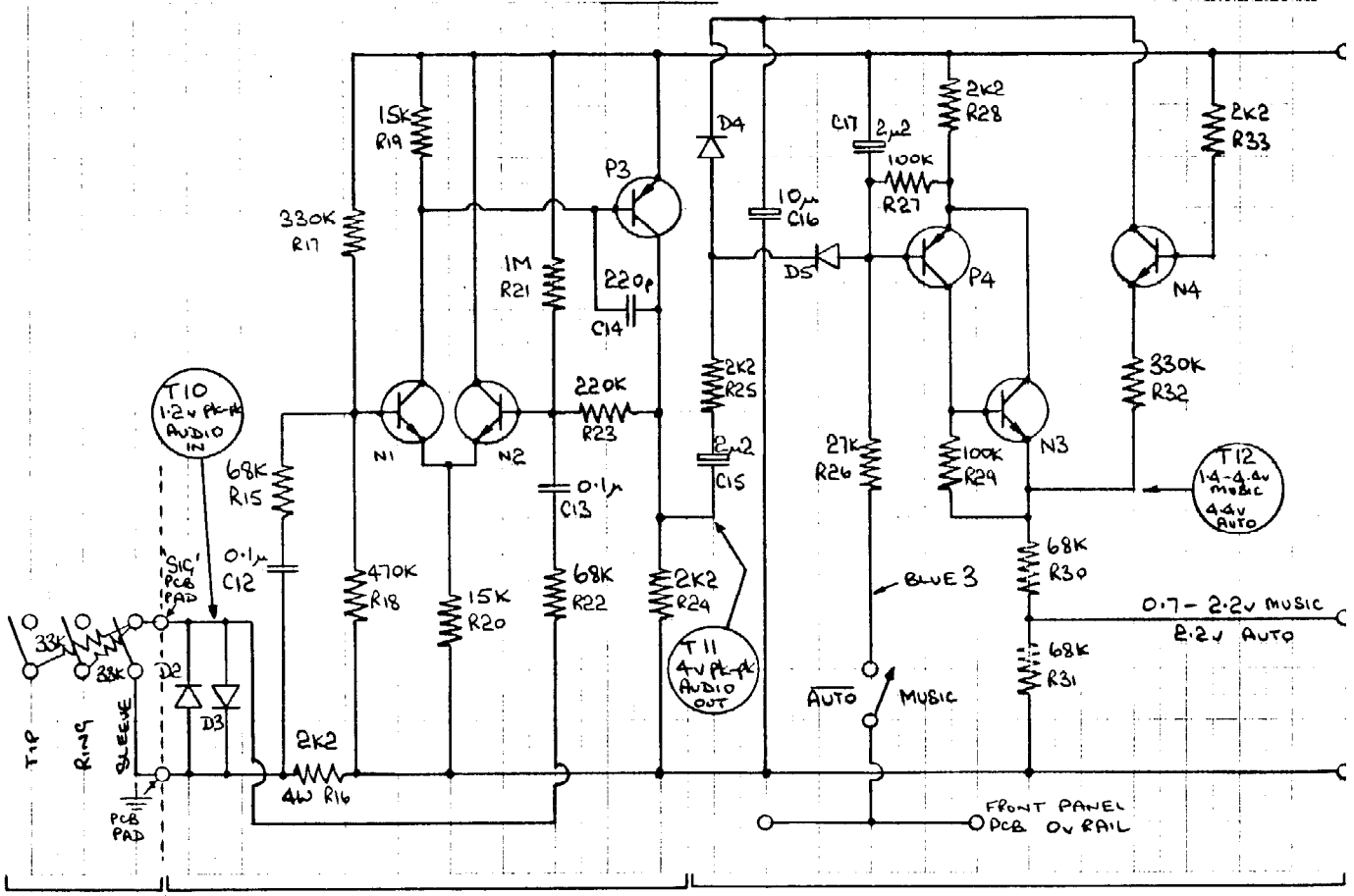
TEN WAY CHASER CIRCUIT DIAGRAM.

P.F



PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM — P.F.M.

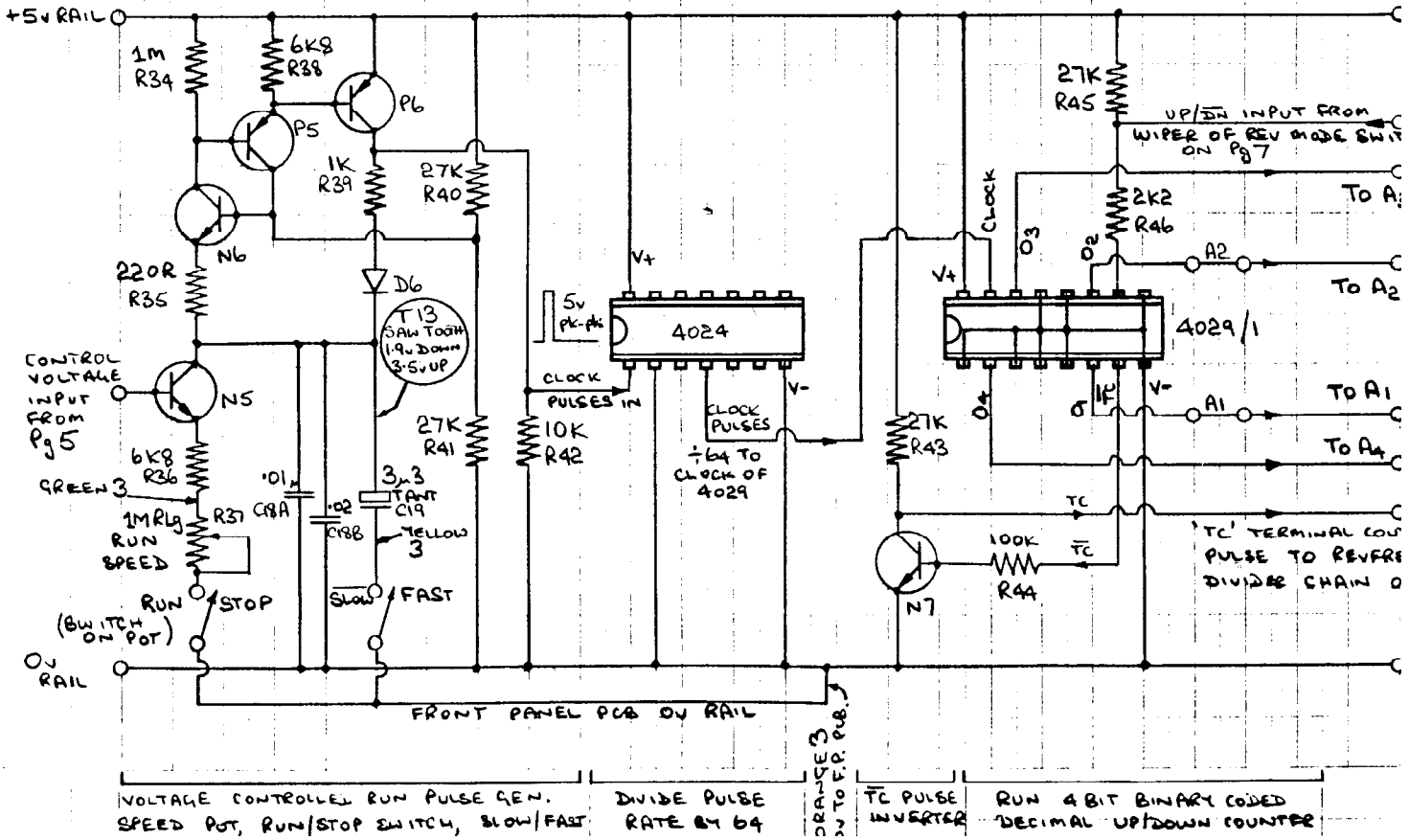
AUDIO



STEREO JACK SOCKET ON BACK PANEL WITH RESISTORS | DIFFERENTIAL LOG AUDIO AMP. | MUSIC/AUTO SWITCH, AUDIO DETECTION AND A.G.C.

PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM — P.F.M

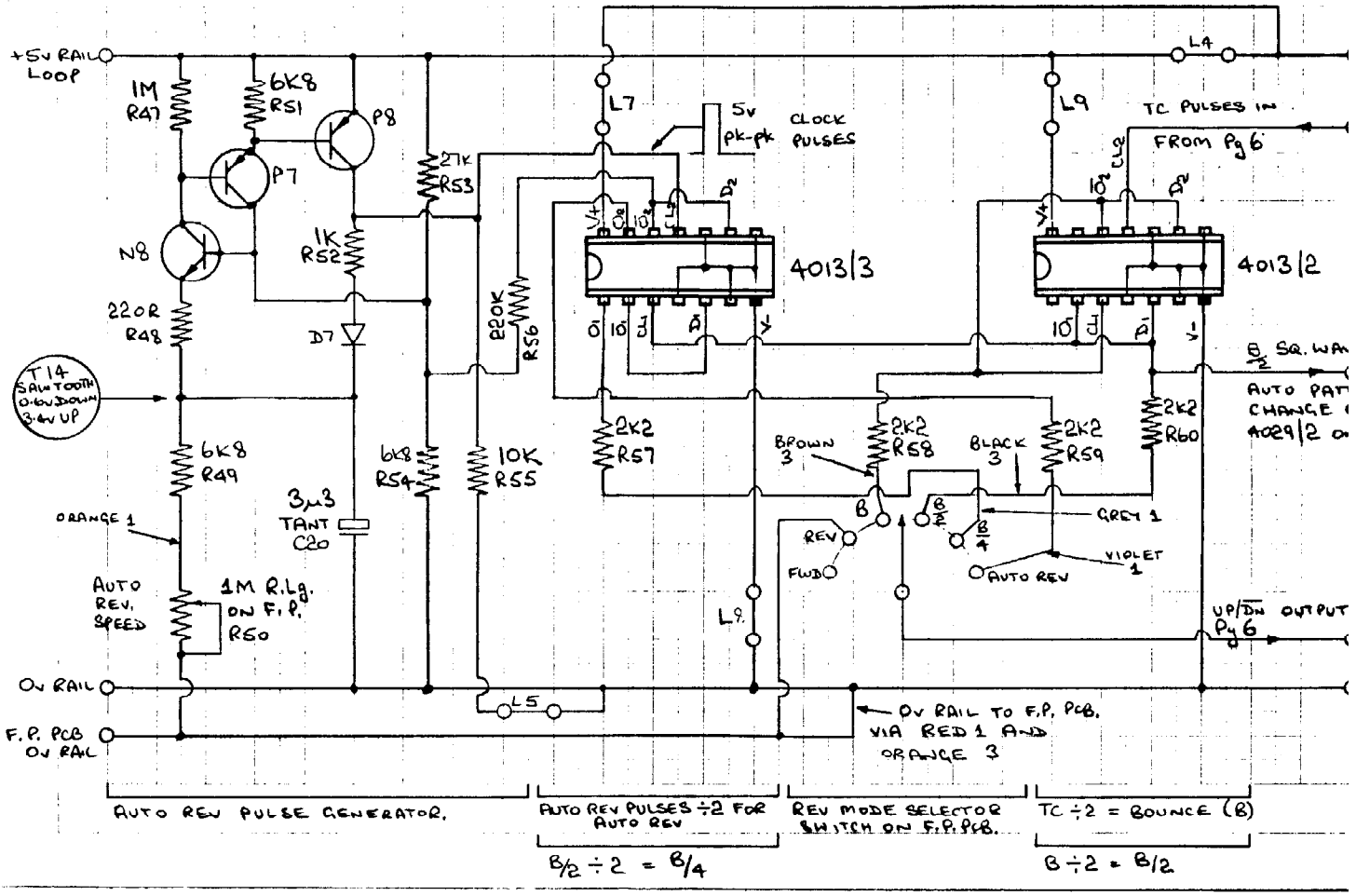
RUN



VOLTAGE CONTROLLED RUN PULSE GEN. SPEED POT, RUN/STOP SWITCH, SLOW/FAST | DIVIDE PULSE RATE BY 64 | TC PULSE INVERTER | RUN 4 BIT BINARY CODED DECIMAL UP/DOWN COUNTER

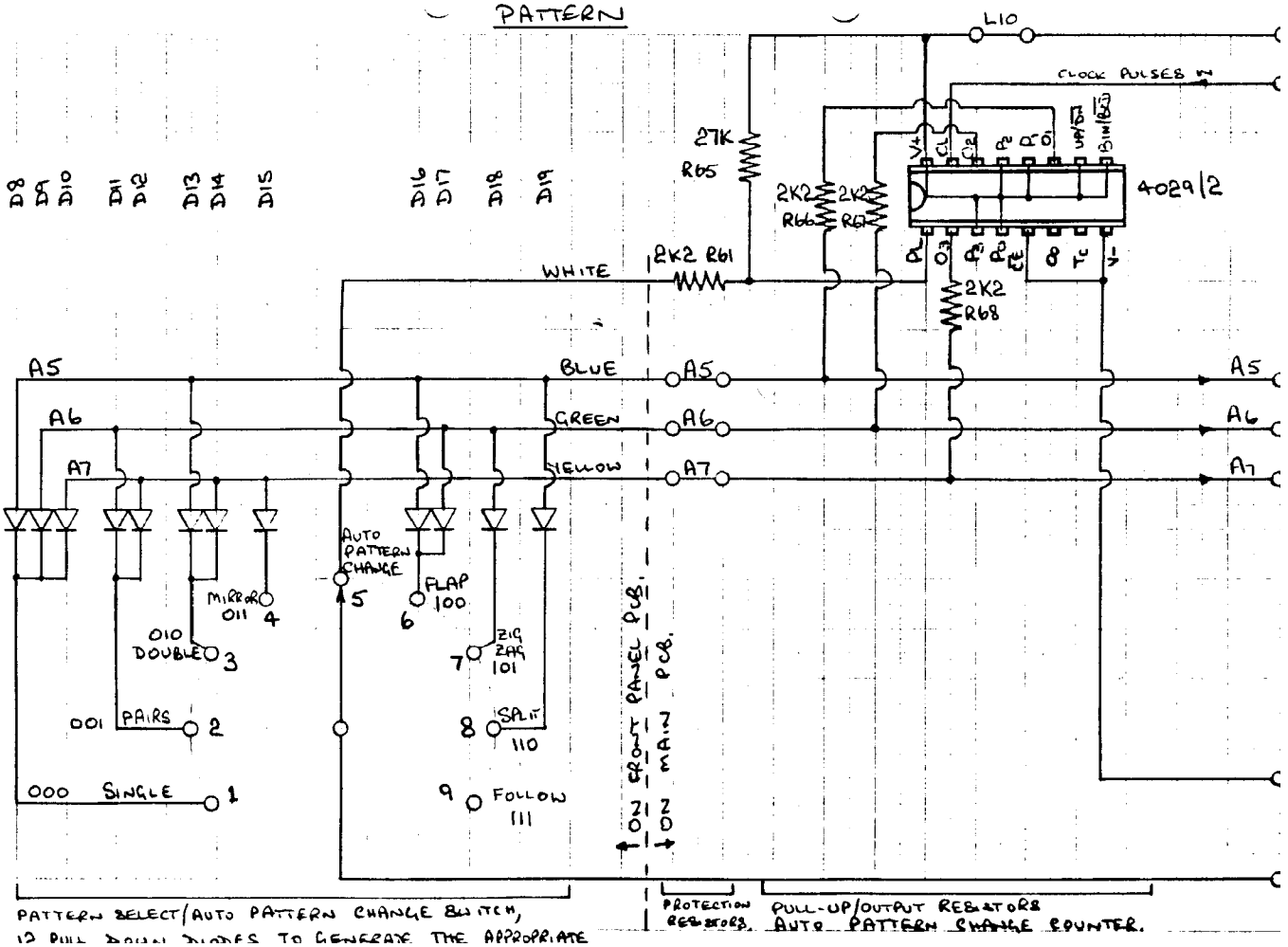
PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM. — P.F.

REVERSING

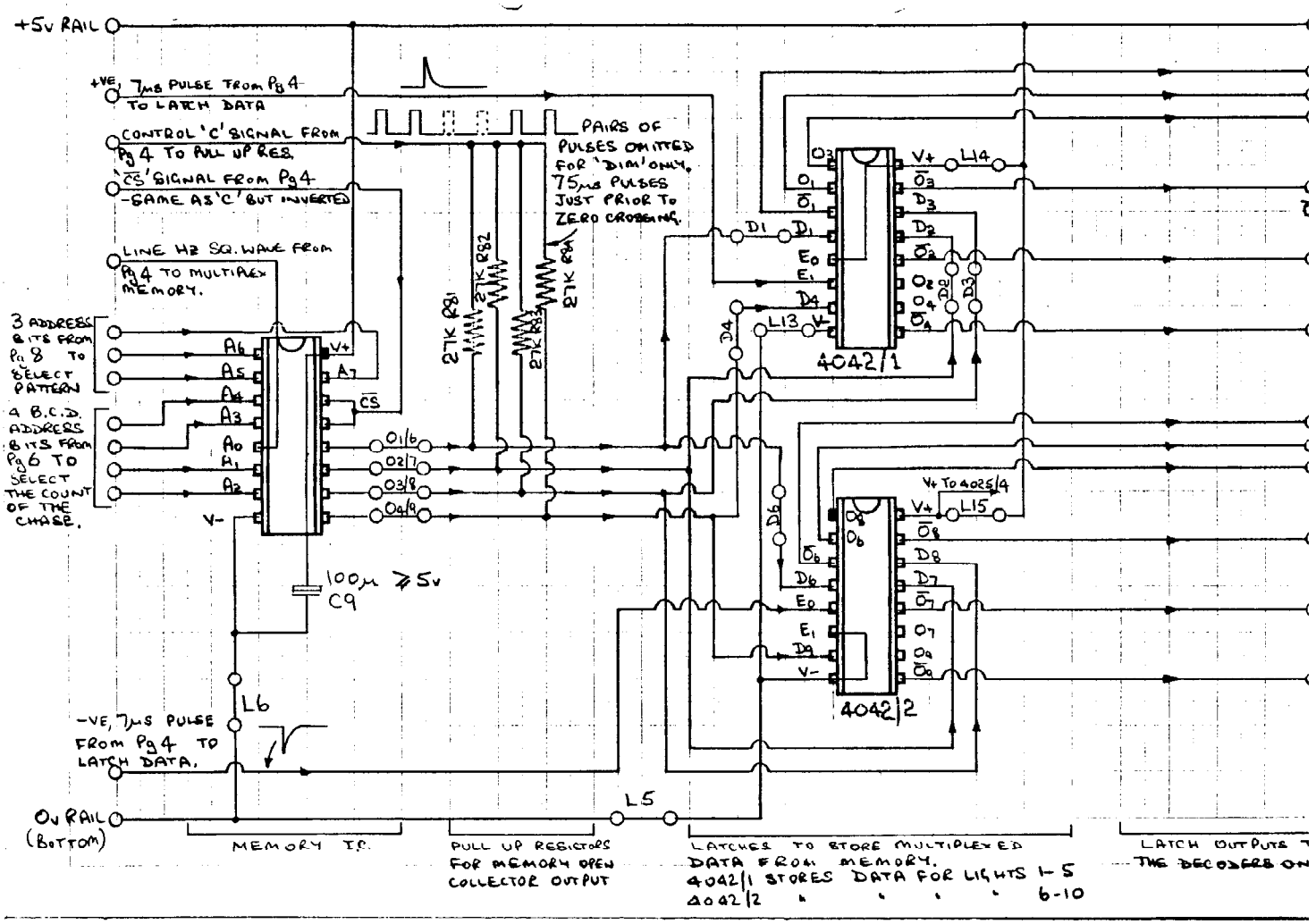


PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM. — P.F.

PATTERN

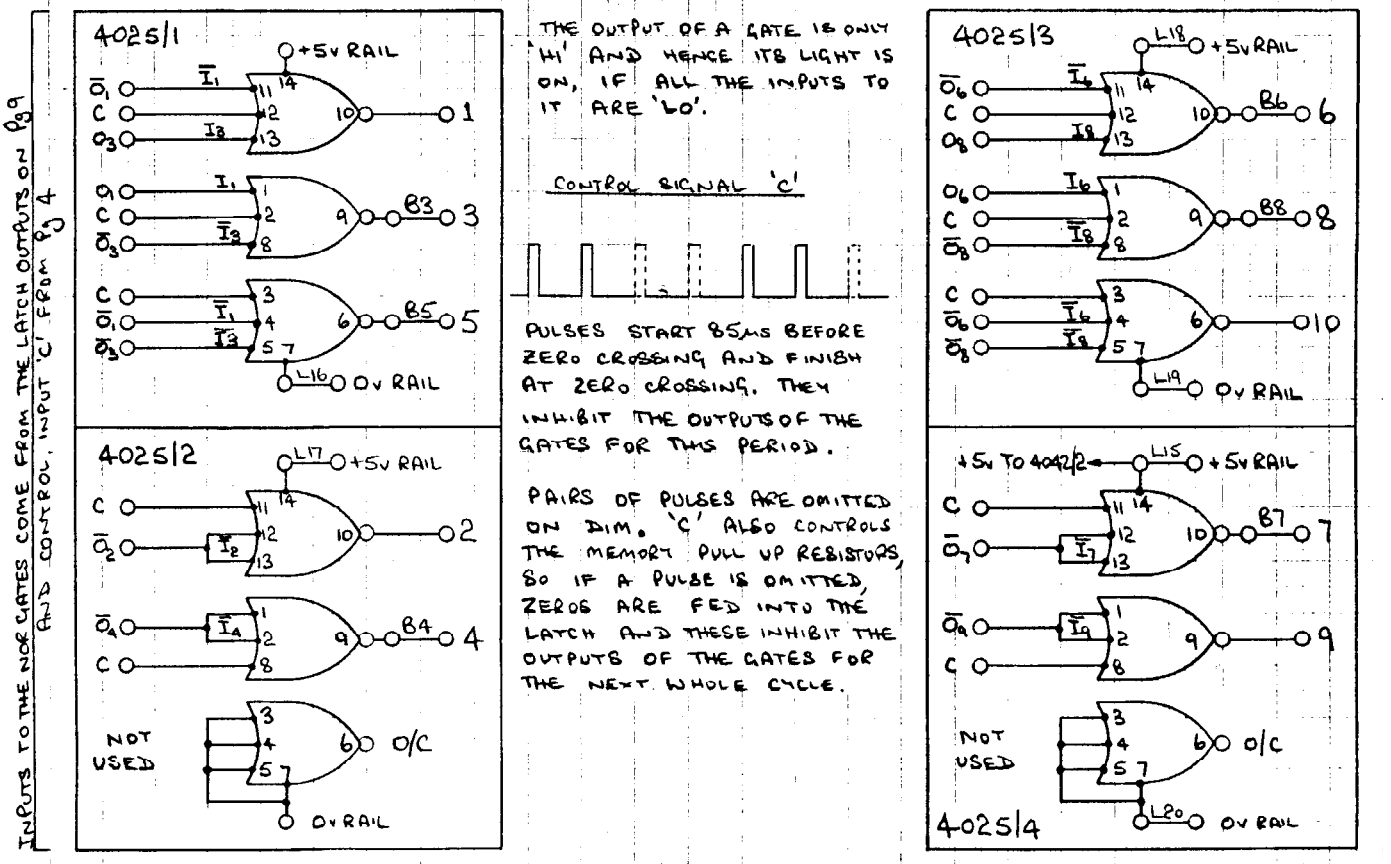


PULBAR — TEN WAY CHASER CIRCUIT DIAGRAM. — P.E.M



PULBAR — TEN WAY CHASER CIRCUIT DIAGRAM. — P.E.M

DECODING



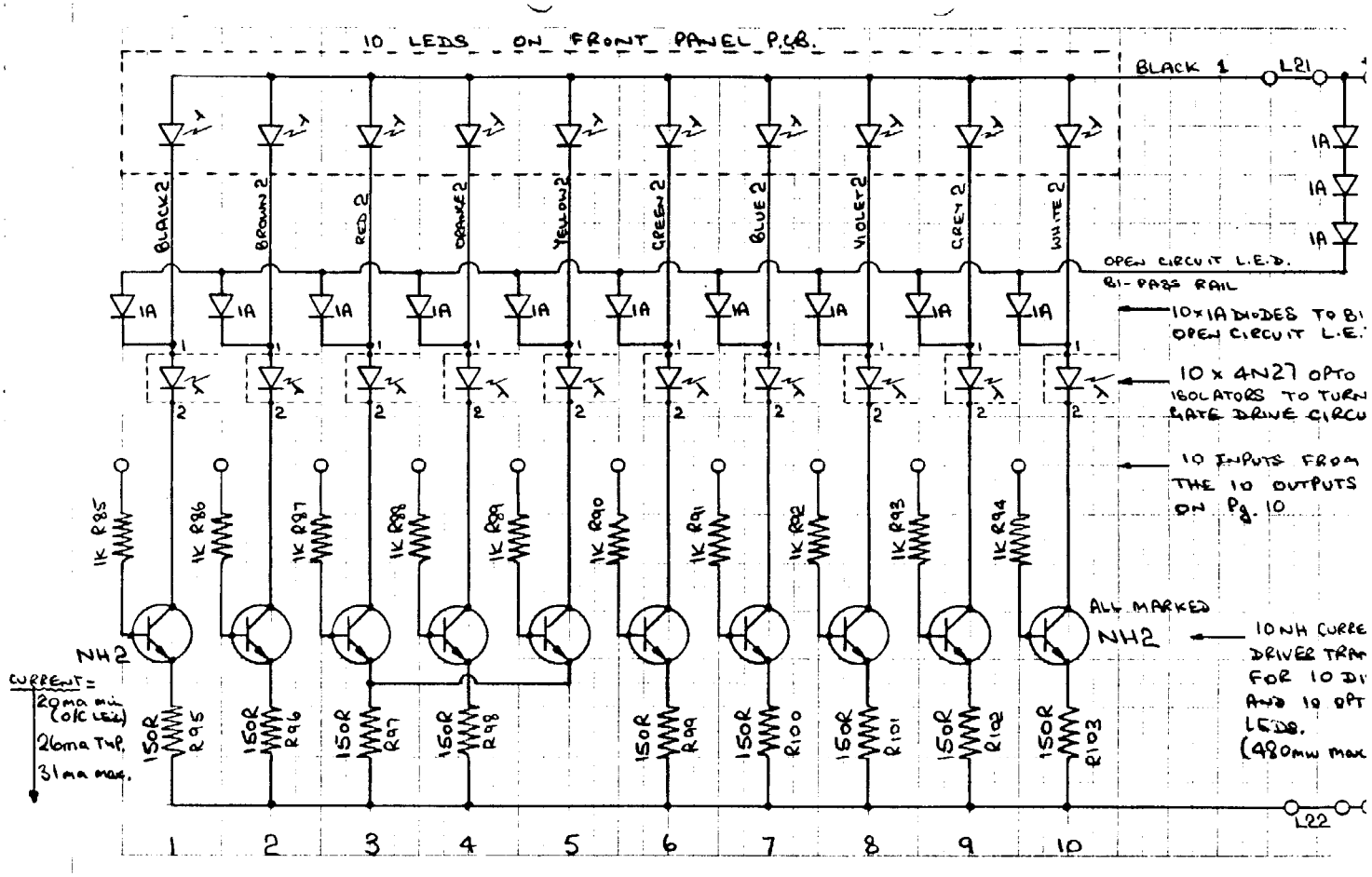
THE OUTPUT OF A GATE IS ONLY 'HI' AND HENCE ITS LIGHT IS ON, IF ALL THE INPUTS TO IT ARE 'LO'.

CONTROL SIGNAL 'C'

PULSES START 85μs BEFORE ZERO CROSSING AND FINISH AT ZERO CROSSING. THEY INHIBIT THE OUTPUTS OF THE GATES FOR THIS PERIOD.

PAIRS OF PULSES ARE OMITTED ON DIM. 'C' ALSO CONTROLS THE MEMORY PULL UP RESISTORS, SO IF A PULSE IS OMITTED, ZEROS ARE FED INTO THE LATCH AND THESE INHIBIT THE OUTPUTS OF THE GATES FOR THE NEXT WHOLE CYCLE.

PULSAR — TEN WAY CHASER CIRCUIT DIAGRAM. — P.F

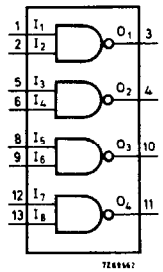


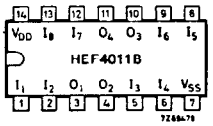
DISPLAY L.E.D.S, OPTO ISOLATOR LEDS, OPEN CIRCUIT LEDS BI-PASS DIODES, CURRENT SOURCE DRIVER T

HEF4011B — HE 11B gates — HE

QUADRUPLE 2-INPUT NAND GATE

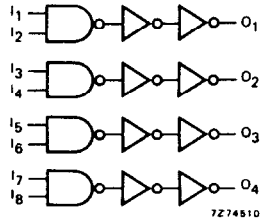
The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4011BP : 14-lead DIL; plastic (SOT-27).
HEF4011BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM

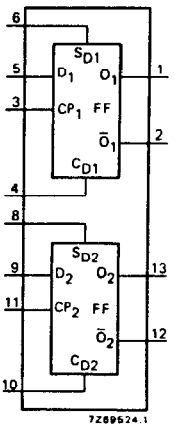


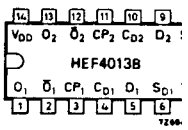
FAMILY DATA

I_{DD} LIMITS category GATES — see Family Specifications

DUAL D-TYPE FLIP-FLOP

The HEF4013B is a dual D-type flip-flop which is edge-triggered and features independent set clear direct, and clock inputs. Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock.
The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and over D or CP inputs. The outputs are buffered for best system performance.





HEF4013BP : 14-lead DIL; plastic (S
HEF4013BD: 14-lead DIL; ceramic (S

TRUTH TABLES

inputs				outputs	
S_D	C_D	CP	D	O	Q̄
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

inputs				outputs	
S_D	C_D	CP	D	O_{n+1}	Q̄
L	L	∫	L	L	
L	L	∫	H	H	

H = HIGH state (the more positive vol
L = LOW state (the less positive voltag
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transitio

PINNING

D data inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
Q̄ complement output

FAMILY DATA

I_{DD} LIMITS category FLIP-FLOPS — see Family Specifications